PROCESS FOR ENHANCEMENT OF VOLTAGE ENDURANCE AND REDUCTION OF PARASITIC CAPACITANCE FOR A TRENCH POWER MOSFET

ABSTRACT OF THE DISCLOSURE

A process for a trench power MOSFET comprises forming a trench on a semiconductor substrate and an oxide and nitride in the trench, etching the oxide and nitride to remain a part of them at the bottom of the trench, and subsequent procedure for the other structure of the trench power MOSFET. Due to the thick insulator formed at the bottom of the trench, the trench power MOSFET is improved by increased voltage endurance and reduced parasitic capacitance, and thereby the cell density is increased.